

REMARKS

The present Amendment amends claims 1, 4-10, 12-14, 16, 17, 19, 21, and 22, and cancels claims 2, 3, 11, 15, 18, and 20. Therefore, the present application has pending claims 1, 4-10, 12-14, 16, 17, 19, 21 and 22.

Specification

The Examiner objected to the title, asserting that it is not descriptive. Applicant has amended the title in accordance with the Examiner's recommendations. Therefore, this objection is overcome and should be withdrawn.

The Examiner objected to the specification, citing informalities. Where appropriate, Applicant has amended the specification. Therefore, this objection is overcome and should be withdrawn.

Drawings

The Examiner objected to Fig. 2 as having an incorrect label. Applicant has amended Fig. 2 in accordance with the Examiner's recommendations. Therefore, this objection is overcome and should be withdrawn.

Claim Objections

The Examiner objected to claims 3, 4, and 18, citing informalities. As indicated above, claims 3 and 18 were canceled. Therefore, this objection with respect to claims 3 and 18 is rendered moot. With regard to claim 4, Applicant has amended claim 4 to overcome the objection. Therefore, this objection should be withdrawn.

35 U.S.C. §101 Rejections

Claims 19-22 stand rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter. As indicated above, claim 20 was canceled. Therefore, this rejection with respect to claim 20 is rendered moot. This rejection with respect to the remaining claims 19, 21 and 22 is traversed for the following reasons. Applicant submits that claims 19, 21 and 22 are now directed to a program executed by a computer. Therefore, this rejection is overcome and should be withdrawn.

35 U.S.C. §112 Rejections

Claims 1-9 and 11-22 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicant regards as the invention. As indicated above, claims 2, 11, 18, and 20 have been canceled. Therefore, this rejection with respect to claims 2, 11, 18, and 20 is rendered moot. This rejection with respect to the remaining claims 1, 3-9, 12-17, 19, 21, and 22 is traversed for the following reasons. Applicants submit that claims 1, 3-9, 12-17, 19, 21, and 22, as now more clearly recited, fully comply with the requirements of 35 U.S.C. §112, second paragraph. Therefore, this rejection is overcome and should be withdrawn.

35 U.S.C. §103 Rejections

Claims 1, 10, 14, and 19

Claims 1, 10, 14, and 19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,526,521 to Lim in view of PowerPath, Version 3.0 Product Guide ("PowerPath"). This rejection is traversed for the following

reasons. Applicant submits that the features of the present invention, as now more clearly recited in claims 1, 10, 14, and 19, are not taught or suggested by either Lim or PowerPath, whether taken individually or in combination with each other as suggested by the Examiner. Therefore, Applicant respectfully requests the Examiner to reconsider and withdraw this rejection.

Amendments were made to the claims to more clearly describe features of the present invention. Specifically, the claims were amended to more clearly describe that the present invention is directed to an information processing system, an information processing apparatus, a control method of changing an information processing apparatus, and a program executed by a computer for controlling an information processing apparatus as recited, for example, in independent claims 1, 10, 14, and 19. Even more specifically, independent claim 1 was amended to include the features of dependent claim 3 (now canceled), and independent claims 10, 14 and 19 were amended to include the features of dependent claims 3 and 4.

The present invention, as recited in independent claim 1 and dependent claim 4, and as similarly recited in claims independent claims 10, 14 and 19, provides an information processing system including a storage having a logical unit logically assigned to a physical device and a plurality of information processing apparatus, which are selectively connected to the storage and that request data input/output from the storage. The information processing system requests data input/output via communications channels to the logical unit. Each of the information processing apparatuses includes an error detection section, a changeover evaluation section,

and a changeover section. The error detection section detects the occurrence of an error on a path according to a result of a data input/output request. The changeover evaluation section detects the occurrence of error on a specified number of paths to determine whether or not to change in information processing apparatus connected to the storage before occurrence of errors on all paths. The changeover section uses a determination result from the changeover evaluation section to change the information processing apparatus requesting data input/output to/from the logical unit. The error detection section also specifies an instantaneous break error resulting from a path's instantaneous break. Furthermore, the changeover evaluation section assigns a larger value to the number of paths used as a criterion for changing an information processing apparatus due to the instantaneous break error than a value assigned to the number of paths used as a criterion for changing an information processing apparatus due to errors other than the instantaneous break error. The information processing system, as recited in dependent claim 4, and as similarly recited in claims 10, 14 and 19, further includes where the error detection section specifies a performance error resulting from path performance degradation. In addition, the changeover evaluation section assigns a smaller value to the number of paths used as criterion for changing an information processing apparatus due to the performance error than a value assigned to the number of paths used as a criterion for performing failover due to errors other than the performance error. The prior art does not disclose all these features.

The above described features of the present invention, as now more clearly recited in the claims, are not taught or suggested by any of the references of record. More specifically, the features are not taught or suggested by either Lim or PowerPath, whether taken individually or in combination with each other in the manner suggested by the Examiner.

Lim discloses a method and apparatus for providing data storage access. However, there is not teaching or suggestion in Lim of the information processing system, the information processing apparatus, the control method of changing an information processing apparatus, or the program executed by a computer for controlling an information processing apparatus, as recited in claims 1, 4, 10, 14, and 19.

The Lim method and apparatus provides access to data storage pathways. The pathways connect a cluster of nodes to a data storage system such that a failover operation can occur from a first node to a second node when the first node suffers pathway degradation forcing the first node to operate significantly slower than it previously operated, even when the first node retains access to the data storage system through one or more available data storage pathways. Such a failover operation from the degraded first node to a second node allows the cluster as a whole to continue performing operations at a rate that is superior to that provided by the degraded first node.

One feature of the present invention, as recited in claim 1 and as similarly recited in claims 10, 14 and 19, includes where the error detection section specifies

an instantaneous break error resulting from a path's instantaneous break. Lim does not disclose this feature. To support the assertion that Lim discloses an error detection section, the Examiner relies upon the detection of unavailable pathways by agents 30, citing column 7, lines 18-51, column 8, lines 8-21, column 10, lines 7-17 and lines 65-67, and column 12, lines 38-40. However, there is no teaching in Lim of where the error detection section specifies an instantaneous break error resulting from a path's instantaneous break, as in the present invention.

Another feature of the present invention, as recited in claim 1 and as similarly recited in claims 10, 14 and 19, includes where the changeover evaluation section assigns a larger value to the number of paths used as a criterion for changing an information processing apparatus due to the instantaneous break error than a value assigned to the number of paths used as a criterion for changing an information processing apparatus due to errors other than the instantaneous break error. Lim does not disclose this feature. To support the assertion that Lim teaches a changeover evaluation section, the Examiner relies upon the cluster framework 28 that executes host failover, citing column 8, lines 55-65 and column 15, lines 1-5. However, there is not teaching in Lim of where the changeover evaluation section assigns a larger value to the number of paths than a value assigned to the number of paths, in the manner claimed.

Yet another feature of the present invention, as recited in claim 4 and as similarly recited in claims 10, 14 and 19, includes where the error detection section specifies a performance error resulting from path performance degradation. Lim

does not disclose this feature. To support the assertion that Lim discloses an error detection section, the Examiner relies upon the detection of unavailable pathways by agents 30, citing column 7, lines 18-51, column 8, lines 8-21, column 10, lines 7-17 and lines 65-67, and column 12, lines 38-40. However, there is no teaching in Lim of where the error detection section specifies a performance error resulting from path performance degradation, as in the present invention.

Still another feature of the present invention, as recited in claim 4 and as similarly recited in claims 10, 14 and 19, includes where the changeover evaluation section assigns a smaller value to the number of paths used as criterion for changing an information processing apparatus due to the performance error than a value assigned to the number of paths used as criterion for performing failover due to errors other than the performance error. Lim does not disclose this feature. To support the assertion that Lim teaches a changeover evaluation section, the Examiner relies upon the cluster framework 28 that executes host failover, citing column 8, lines 55-65 and column 15, lines 1-5. However, there is not teaching in Lim of where the changeover evaluation section assigns a smaller value to the number of paths than a value assigned to the number of paths, in the manner claimed.

Therefore, Lim fails to teach or suggest "said error detection section specifies an instantaneous break error resulting from a path's instantaneous break" as recited in claim 1, and as similarly recited in claims 10, 14 and 19.

Furthermore, Lim fails to teach or suggest “said changeover evaluation section assigns a larger value to the number of paths used as a criterion for changing an information processing apparatus due to said instantaneous break error than a value assigned to the number of paths used as a criterion for changing an information processing apparatus due to errors other than the instantaneous break error” as recited in claim 1, and as similarly recited in claims 10, 14 and 19.

Even further, Lim fails to teach or suggest where “said error detection section specifies a performance error resulting from path performance degradation” as recited in claim 4, and as similarly recited in claims 10, 14 and 19.

Yet even further, Lim fails to teach or suggest where “said changeover evaluation section assigns a smaller value to the number of paths used as a criterion for changing an information processing apparatus due to said performance error than a value assigned to the number of paths used as a criterion for performing failover due to errors other than the performance error” as recited in claim 4, and as similarly recited in claims 10, 14 and 19.

The above noted deficiencies of Lim are not supplied by any of the other references, particularly PowerPath. Therefore, combining the teachings of PowerPath with Lim still fails to teach or suggest the features of the present invention, as now more clearly recited in the claims.

PowerPath discloses host-based software that works with storage systems to intelligently manage input/output paths. However, there is no teaching or suggestion in PowerPath of the information processing system, the information processing

apparatus, the control method of changing an information processing apparatus, or the program executed by a computer for controlling an information processing apparatus, as recited in claims 1, 4, 10, 14, and 19.

The PowerPath software works with storage systems to intelligently manage I/O paths. It supports multi-channel access to logical devices. Furthermore, the software dynamically load balances I/O requests, and automatically detects and recovers from path failures.

One feature of the present invention, as recited in claim 1 and as similarly recited in claims 10, 14 and 19, includes where the error detection section specifies an instantaneous break error resulting from a path's instantaneous break. PowerPath does not disclose this feature. As described on page 2-2, PowerPath merely discloses an automatic path failover feature that automatically redirects data from a failed I/O path to an alternate path. There is not disclosure in PowerPath of where the error detection section specifies an instantaneous break error resulting from a path's instantaneous break, as in the present invention.

Another feature of the present invention, as recited in claim 1 and as similarly recited in claims 10, 14 and 19, includes where the changeover evaluation section assigns a larger value to the number of paths used a criterion for changing an information processing apparatus due to the instantaneous break error than a value assigned to the number of paths used as a criterion for changing an information processing apparatus due to errors other than the instantaneous break error. PowerPath does not disclose this feature. As described on page 2-2, PowerPath

discloses dynamic multipath load balancing and automatic path failover. However, PowerPath does not disclose where a changeover evaluation section assigns a larger value to the number of paths than a value assigned to the number of paths, as in the present invention.

Yet another feature of the present invention, as recited in claim 4 and as similarly recited in claims 10, 14 and 19, includes where the error detection section specifies a performance error resulting from path performance degradation. PowerPath does not disclose this feature. As described on page 2-2, PowerPath merely discloses an automatic path failover feature that automatically redirects data from a failed I/O path to an alternate path. There is not disclosure in PowerPath of where the error detection section specifies a performance error resulting from path performance degradation, as in the present invention.

Still another feature of the present invention, as recited in claim 4 and as similarly recited in claims 10, 14 and 19, includes where the changeover evaluation section assigns a smaller value to the number of paths used as criterion for changing an information processing apparatus due to the performance error than a value assigned to the number of paths used as criterion for performing failover due to errors other than the performance error. PowerPath does not disclose this feature. As described on page 2-2, PowerPath discloses dynamic multipath load balancing and automatic path failover. However, PowerPath does not disclose where a changeover evaluation section assigns a smaller value to the number of paths than a value assigned to the number of paths, as in the present invention.

Therefore, PowerPath fails to teach or suggest “said error detection section specifies an instantaneous break error resulting from a path’s instantaneous break” as recited in claim 1, and as similarly recited in claims 10, 14 and 19.

Furthermore, PowerPath fails to teach or suggest “said changeover evaluation section assigns a larger value to the number of paths used as a criterion for changing an information processing apparatus due to said instantaneous break error than a value assigned to the number of paths used as a criterion for changing an information processing apparatus due to errors other than the instantaneous break error” as recited in claim 1, and as similarly recited in claims 10, 14 and 19.

Even further, PowerPath fails to teach or suggest where “said error detection section specifies a performance error resulting from path performance degradation” as recited in claim 4, and as similarly recited in claims 10, 14 and 19.

Yet even further, PowerPath fails to teach or suggest where “said changeover evaluation section assigns a smaller value to the number of paths used as a criterion for changing an information processing apparatus due to said performance error than a value assigned to the number of paths used as a criterion for performing failover due to errors other than the performance error” as recited in claim 4, and as similarly recited in claims 10, 14 and 19.

Both Lim and PowerPath suffer from the same deficiencies relative to the features of the present invention, as recited in the claims. Therefore, combining the teachings of Lim and PowerPath in the manner suggested by the Examiner does not render obvious the features of the present invention, as now more clearly recited in

claims 1, 10, 14, and 19. Accordingly, reconsideration and withdrawal of the 35 U.S.C. §103(a) rejection of claims 1, 10, 14, and 19 as being unpatentable over Lim in view of PowerPath is respectfully requested.

The remaining references of record have been studied. Applicant submits that they do not supply any of the deficiencies noted above with respect to the references used in the rejection of claims 1, 10, 14, and 19.

Claims 5, 6, 9, 12, 16, and 21

Claims 2, 5, 6, 9, 11, 12, 15, 16, 20, and 21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Lim in view of PowerPath, further in view of U.S. Patent No. 6,145,028 to Shank, et al. ("Shank"). As indicated above, claims 2, 11, 15, and 20 were canceled. Therefore, this rejection with respect to claims 2, 11, 15, and 20 is rendered moot. This rejection with respect to the remaining claims 5, 6, 9, 12, 16, and 21 is traversed for the following reasons. Applicants submit that the features of claims 5, 6, 9, 12, 16, and 21, as now more clearly recited, are not taught or suggested by Lim, PowerPath, or Shank, whether taken individually, or in combination with each other in the manner suggested by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Amendments were made to the claims to more clearly describe features of the present invention. Specifically, the claims were amended to more clearly describe that the present invention is directed to an information processing system, an information processing apparatus, a control method of changing an information

processing apparatus, and a program executed by a computer for controlling an information processing apparatus as recited, for example, in independent claim 9 and dependent claims 5, 6, 12, 16, and 21. Even more specifically, independent claim 9 was amended to include the features of dependent claims 3 (now canceled) and 4.

Regarding dependent claims 5, 6, 12, 16, and 21, claims 5 and 6 are dependent on claim 1, claim 12 is dependent on claim 10, claim 16 is dependent on claim 14, and claim 21 is dependent on claim 19. Therefore, Applicant submits that dependent claims 5, 6, 12, 16, and 21 are patentable for at least the reasons previously discussed regarding independent claims 1, 10, 14, and 19.

Regarding independent claim 9, the present invention, as described in claim 9, provides an information processing system including a storage having a logical unit logically assigned to a physical device, and a plurality of information processing apparatuses. The information processing apparatus are selectively connected to the storage and request data input/output from the storage. The information processing system requests data input/output via a communication channel to the logical unit. Each of the information processing apparatuses includes a path selection section that selects a path assigned with a data input/output request transmitted to the storage, and an input/output transmission/reception section that transmits a data input/output request issued to a path selected by the path selection section. Each of the information processing apparatuses further includes an operation statistics management section that totals process states of normally terminated data

input/output requests, and an error management section that detects the occurrence of an error for each path and error type. Also included in each of the information processing apparatuses is a changeover evaluation section that detects occurrence of error on a specified number of paths to determine whether or not to change an information processing apparatus connected to the storage, even before the occurrence of errors on all paths. Furthermore, each of the information processing apparatuses includes a changeover section that uses a determination result from the changeover evaluation section to change the information processing apparatus requested data input/output to/from the logical unit. In the information processing system, the error management section specifies an instantaneous break error resulting from a path's instantaneous break and a performance error resulting from performance degradation. The changeover evaluation section assigns a larger value to the number of paths used as a criterion for changing an information processing apparatus due to the instantaneous break error than a value assigned to the number of paths used as a criterion for changing an information processing apparatus due to errors other than the instantaneous break error. In addition, the changeover evaluation section assigns a smaller value to the number of paths used as a criterion for changing an information processing apparatus due to the performance error than a value assigned to the number of paths used as a criterion for performing failover due to errors other than the performance error. The prior art does not disclose all these features.

The above described features of the present invention, as now more clearly recited in the claims, are not taught or suggested by any of the references of record. More specifically, the features are not taught or suggested by Lim, PowerPath or Shank, whether taken individually or in combination with each other in the manner suggested by the Examiner.

As previously discussed, Lim discloses a method and apparatus for providing data storage access. However, there is not teaching or suggestion in Lim of the information processing system, as recited in claim 9.

One feature of the present invention, as recited in claim 9, includes where the error management section specifies an instantaneous break error resulting from a path's instantaneous break and a performance error resulting from path performance degradation. Lim does not disclose this feature. As conceded by the Examiner, Lim does not disclose an error management section. Therefore, Lim fails to teach where an error management section specifies an instantaneous break error resulting from a path's instantaneous break and a performance error resulting from path performance degradation, as in the present invention.

Another feature of the present invention, as recited in claim 9 includes where the changeover evaluation section assigns a larger value to the number of paths used a criterion for changing an information processing apparatus due to the instantaneous break error than a value assigned to the number of paths used as a criterion for changing an information processing apparatus due to errors other than the instantaneous break error. Lim does not disclose this feature. To support the

assertion that Lim discloses a changeover evaluation section, the Examiner relies upon the cluster framework 28 executing a host failover, citing column 8, lines 55-65 and column 15, lines 1-5. However, there is no teaching or suggestion in Lim of where the changeover evaluation section assigns a larger value to the number of paths than a value assigned to the number of paths, as in the present invention.

Yet another feature of the present invention, as recited in claim 9 includes where the changeover evaluation section assigns a smaller value to the number of paths used as criterion for changing an information processing apparatus due to the performance error than a value assigned to the number of paths used as criterion for performing failover due to errors other than the performance error. Lim does not disclose this feature. To support the assertion that Lim discloses a changeover evaluation section, the Examiner relies upon the cluster framework 28 executing a host failover, citing column 8, lines 55-65 and column 15, lines 1-5. However, there is no teaching or suggestion in Lim of where the changeover evaluation section assigns a smaller value to the number of paths than a value assigned to the number of paths, as in the present invention.

Therefore, Lim fails to teach or suggest “said error management section specifies an instantaneous break error resulting from a path’s instantaneous break and performance error resulting from path performance degradation” as recited in claim 9.

Furthermore, Lim fails to teach or suggest “said changeover evaluation section assigns a larger value to the number of paths used as a criterion for

changing an information processing apparatus due to said instantaneous break error than a value assigned to the number of paths used as a criterion for changing an information processing apparatus due to errors other than the instantaneous break error” as recited in claim 9.

Even further, Lim fails to teach or suggest where “said changeover evaluation section assigns a smaller value to the number of paths used as a criterion for changing an information processing apparatus due to said performance error than a value assigned to the number of paths used as a criterion for performing failover due to errors other than the performance error” as recited in claim 9.

The above noted deficiencies of Lim are not supplied by any of the other references, particularly PowerPath. Therefore, combining the teachings of PowerPath with Lim still fails to teach or suggest the features of the present invention, as now more clearly recited in the claims.

As previously discussed, PowerPath discloses host-based software that works with storage systems to intelligently manage input/output paths. However, there is no teaching or suggestion in PowerPath of the information processing system, as recited in claim 9.

One feature of the present invention, as recited in claim 9, includes where the error management section specifies an instantaneous break error resulting from a path’s instantaneous break and a performance error resulting from path performance degradation. PowerPath does not disclose this feature. As described on page 2-2, PowerPath merely discloses an automatic path failover feature that automatically

redirects data from a failed I/O path to an alternate path. There is not disclosure in PowerPath of where the error management section specifies an instantaneous break error resulting from a path's instantaneous break and a performance error resulting from path performance degradation, as in the present invention.

Another feature of the present invention, as recited in claim 9 includes where the changeover evaluation section assigns a larger value to the number of paths used as a criterion for changing an information processing apparatus due to the instantaneous break error than a value assigned to the number of paths used as a criterion for changing an information processing apparatus due to errors other than the instantaneous break error. PowerPath does not disclose this feature. As described on page 2-2, PowerPath discloses dynamic multipath load balancing and automatic path failover. However, PowerPath does not disclose where a changeover evaluation section assigns a larger value to the number of paths than a value assigned to the number of paths, as in the present invention.

Yet another feature of the present invention, as recited in claim 9 includes where the changeover evaluation section assigns a smaller value to the number of paths used as criterion for changing an information processing apparatus due to the performance error than a value assigned to the number of paths used as criterion for performing failover due to errors other than the performance error. PowerPath does not disclose this feature. As described on page 2-2, PowerPath discloses dynamic multipath load balancing and automatic path failover. However, PowerPath does not disclose where a changeover evaluation section assigns a smaller value to the

number of paths than a value assigned to the number of paths, as in the present invention.

Therefore, PowerPath fails to teach or suggest “said error management section specifies an instantaneous break error resulting from a path’s instantaneous break and performance error resulting from path performance degradation” as recited in claim 9.

Furthermore, PowerPath fails to teach or suggest “said changeover evaluation section assigns a larger value to the number of paths used as a criterion for changing an information processing apparatus due to said instantaneous break error than a value assigned to the number of paths used as a criterion for changing an information processing apparatus due to errors other than the instantaneous break error” as recited in claim 9.

Even further, PowerPath fails to teach or suggest where “said changeover evaluation section assigns a smaller value to the number of paths used as a criterion for changing an information processing apparatus due to said performance error than a value assigned to the number of paths used as a criterion for performing failover due to errors other than the performance error” as recited in claim 9.

The above noted deficiencies of Lim and PowerPath are not supplied by any of the other references, particularly Shank. Therefore, combining the teachings of Shank with Lim and PowerPath still fails to teach or suggest the features of the present invention, as now more clearly recited in the claims.

Shank discloses a method and apparatus for enhanced multi-pathing to an array of storage devices. However, there is no teaching or suggestion in Shank of the information processing apparatus, the control method of changing an information processing apparatus, or the program executed by a computer for controlling an information processing apparatus, as recited in claim 9.

Shank teaches a method of multi-pathing to an array of storage devices. The method includes scanning the array of storage devices to find available I/O paths, storing a list of available I/O paths to each storage device in a memory, and receiving an I/O request directed at a virtual disk memory location. The method also includes mapping the virtual disk memory location to a corresponding storage device and selecting an I/O path for the I/O request from the list of available I/O paths stored in the memory. Furthermore, the method includes transmitting the I/O request to the storage device over the selected I/O path. The Shank apparatus includes a virtual disk driver functionally coupled between the computer and the disk array with a core driver and a subordinate driver customized for storage device arrays from different hardware vendors. Selection of the subordinate driver is accomplished via a switch table stored in the computer memory.

One feature of the present invention, as recited in claim 9, includes where the error management section specifies an instantaneous break error resulting from a path's instantaneous break and a performance error resulting from path performance degradation. Shank does not disclose this feature. The Examiner relies upon Shank for teaching an error management section, citing column 7, lines 45-51. However,

there is no teaching or disclosure in Shank of where the error management specifies an instantaneous break error resulting from a path's instantaneous break and a performance error resulting from path performance degradation, as in the present invention.

Another feature of the present invention, as recited in claim 9 includes where the changeover evaluation section assigns a larger value to the number of paths used a criterion for changing an information processing apparatus due to the instantaneous break error than a value assigned to the number of paths used as a criterion for changing an information processing apparatus due to errors other than the instantaneous break error. Shank does not disclose this feature, and the Examiner does not rely upon Shank for disclosing this feature.

Yet another feature of the present invention, as recited in claim 9 includes where the changeover evaluation section assigns a smaller value to the number of paths used as criterion for changing an information processing apparatus due to the performance error than a value assigned to the number of paths used as criterion for performing failover due to errors other than the performance error. Shank does not disclose this feature, and the Examiner does not rely upon Shank for disclosing this feature.

Therefore, Shank fails to teach or suggest "said error management section specifies an instantaneous break error resulting from a path's instantaneous break and performance error resulting from path performance degradation" as recited in claim 9.

Furthermore, Shank fails to teach or suggest “said changeover evaluation section assigns a larger value to the number of paths used as a criterion for changing an information processing apparatus due to said instantaneous break error than a value assigned to the number of paths used as a criterion for changing an information processing apparatus due to errors other than the instantaneous break error” as recited in claim 9.

Even further, Shank fails to teach or suggest where “said changeover evaluation section assigns a smaller value to the number of paths used as a criterion for changing an information processing apparatus due to said performance error than a value assigned to the number of paths used as a criterion for performing failover due to errors other than the performance error” as recited in claim 9.

Lim, PowerPath and Shank each suffer from the same deficiencies relative to the features of the present invention, as recited in the claims. Therefore, combining the teachings of Lim, PowerPath and Shank in the manner suggested by the Examiner does not render obvious the features of the present invention, as now more clearly recited in claims 5, 6, 9, 12, 16, and 21. Accordingly, reconsideration and withdrawal of the 35 U.S.C. §103(a) rejection of claims 5, 6, 9, 12, 16, and 21 as being unpatentable over Lim in view of PowerPath, further in view of Shank is respectfully requested.

The remaining references of record have been studied. Applicant submits that they do not supply any of the deficiencies noted above with respect to the references used in the rejection of claims 5, 6, 9, 12, 16, and 21.

Claims 4, 7, 8, 13, 17, and 22

Regarding dependent claims 4, 7, 8, 13, 17, and 22, it should be noted that the Examiner did not provide any prior art rejections for these claims. Applicant has reviewed the references of record, and submits that the features of the present invention, as recited in claims 4, 7, 8, 13, 17, and 22, are not taught or suggested by any of the references of record, whether taken alone or in combination with each other.

In view of the foregoing amendments and remarks, Applicant submits that claims 1, 4-10, 12-14, 16, 17, 19, 21, and 22 are in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Mattingly, Stanger, Malur & Brundidge, P.C., Deposit Account No. 50-1417 (referencing attorney docket no. 1213.43684X00).

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.



Carl I. Brundidge
Registration No. 29,621

CIB/DKM/sdb
(703) 684-1120
Attachment:

Replacement Sheet (Fig. 2)

Amendments to the Drawings

The attached sheet of drawings includes changes to Fig. 2. In Fig. 2, #140, "1F" is changed to "IF".